Synopsys Timing Constraints And Optimization User Guide

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Synopsys Timing Constraints And Optimization

Synopsys Timing Constraints and Optimization User Guide
Synopsys® Timing Constraints and Optimization User Guide Version D-201003, March 2010
A Power-Centric Timing Optimization Flow - Synopsys
– Available now via SolvNet for joint Synopsys and ARM customers 1 “big” cluster: dual-core Cortex-A15 processor – Scripts, design information, documentation
DC Ultra - Synopsys
synopsyscom Overview • Concurrent optimization of timing, area, power and test prioritizes design rule requirements over timing and area constraints By setting the appropriate priority, designers can drive synthesis to achieve the best QoR for a design Compile directives in DC Ultra can be used to further control optimization
Using the Synopsys Design Constraints Format Application Note
Using the Synopsys Design Constraints Format 1 Synopsys Design Constraints (SDC) is a format used to specify the design intent, including the timing, power, and area constraints for a design SDC is based on the tool command language (Tcl) The Synopsys Design Compiler, IC Compiler, and PrimeTime tools use the
RTL-to-Gates Synthesis using Synopsys Design Compiler
Synopsys Design Compiler to elaborate RTL, set optimization constraints, synthesize to gates, and prepare various area and timing reports You will

also learn how to read the various DC text reports and how to use the graphical Synopsys Design Vision tool to visualize the synthesized design

RTL-to-Gates Synthesis using Synopsys Design Compiler

meet timing and ultimately fail If the period is too large, then the tools will have no trouble but you will get a very conservative implementation For more information about constraints consult the Synopsys Timing Constraints and Optimization User Guide (dc-user-guide-tcopdf) dc_shell> create_clock clk -name ideal_clock1 -period 2

Synopsys Synplify Support

• Verilog Quartus Mapping File (vqm) netlist• The Synopsys Constraints Format (scf) file for TimeQuest Timing Analyzer constraints• Thetcl file to set up your Quartus II project and pass constraints Note: Alternatively, you can run the Quartus II software from within the Synplify software 6 After obtaining place-and-route results that meet your requirements, configure or program

Automated Synthesis from HDL models

Automated Synthesis from HDL models Design Compiler (Synopsys) Leonardo (Mentor Graphics) Design optimization constraints: user-specified timing and area optimization goals DC tries to optimize these without violating design rules Common constraints: timing and area

Chapter 9 Design Constraints and Optimization

Timing constraints are used to specify the timing characteristics of the design Timing constraints may affect all internal timing interconnections, delays through logic and LUTs and between flip-flops or registers Timing constraints can be either global or path-specific Design Constraints and Optimization On-chip routing resources

Design Constraints User's Guide

Timing Constraints Timing constraints represent the performance goals for your designs Designer software uses timing constraints to guide the timing-driven optimization tools in order to meet these goals You can set timing constraints either globally or to a specific set of paths in your design You can apply timing constraints to:

RTL-to-Gates Synthesis using Synopsys Design Compiler

divisor (GCD) cicruit, set optimization constraints, synthesize the design to gates, and prepare various area and timing reports You will also learn how to read the various DC text reports and how to use the graphical Synopsys Design Vision tool to visualize the synthesized design Note that this tutorial is by no means comprehensive

RTL-to-Gates Synthesis using Synopsys Design Compiler

use Synopsys Design Compiler to elaborate RTL, set optimization constraints, synthesize to gates, and prepare various area and timing reports Synopsys provides a library called Design Ware which includes highly optimized RTL for arithmetic building blocks For example, the Design Ware libraries contain adders, multipliers, comparators, and

Xilinx Synopsys Interface EPLD User Guide

Synopsys Design Compiler Timing and resource utilization results are available from XEPLD after completion of fitting (fitnet) The XEPLD fitter (v50) currently does not support timing-constraint-driven optimization; Synopsys timing constraints have no effect on …

Design Constraints User Guide

The Libero SoC software supports both SDC timing and PDC physical constraints In addition, it supports netlist optimization constraints You can set constraints by either using Microsemi's interactive tools (I/O Editor, Chip Planner, and Constraint Editor) or by

Quartus II Handbook Volume 2: Design Implementation and ...

User-created constraints are contained in one of two files: the Quartus II Settings File (qsf) or, in the case of timing constraints, the Synopsys Design Constraints file (sdc) Constraints and assignments made with the Device dialog box, Settings dialog box, Assignment Editor, Chip Planner, and Pin

Vivado Design Suite User Guide

device resources, within the logical, physical, and timing constraints of the design For more information about the design flow s supported by the Vivado tools, see the Vivado Design Suite User Guide: Design Flows Overview (UG892) [Ref 1] SDC and XDC Constraint Support The Vivado Design Suite implementation is a timing-driven flow

ECE 128 Synopsys Tutorial: Using the Design Compiler ...

Optimization Gate Level Simulation Static Timing Analysis Place and Route Static Timing Analysis Preliminary Netlist Handoff In this tutorial, we will be working in “Logic Synthesis” portion of the ASIC flow In this course, we will use the Synopsys Product Family for synthesis IN particular, we will concentrate on the Synopsys Tool called the

Synopsys FPGA Synthesis

Synopsys FPGA Synthesis Synplify Pro Tutorial March 2010 chical Optimization Technology, High -performance ASIC Prototyping System, HSIM, HSIMplus, i-Virtual Stepper, IICE, timing constraints The constraint file will be created using this tutorial However, you can

SmartFusion2/IGLOO2 FPGA Timing Constraints User’s Guide

Libero tools (Timing Driven Place and Route and SmartTime) support a subset of Synopsys SDC timing constraints relevant for FPGA designs Microsemi recommends that you create two sets of timing constraints in the Libero flow • FDC timing constraints for synthesis with Synplify Pro